Amendments to the Drawings:

The attached drawing sheet(s) include no changes to Figure(s) 1-6. The three original drawing sheets are amended to revise the numbering of the drawing sheets. In particular, the first drawing sheet is amended to refer to drawing sheet 1 of 4. Likewise, the second and third drawing sheets are amended to refer to drawing sheets 2 and 3 of 4, respectively. Additionally, drawing sheet 4 is added to add an additional Figure. Specifically, Figure 7 is added to depict one embodiment of the integrated circuit chip 200. The addition of Figure 7 is supported, for example, by the subject matter described in the original specification on page 2, line 32, through page 3, line 15, and in the original language of claims 1 and 2.

REMARKS/ARGUMENTS

In the Office Action mailed March 11, 2008, claims 1-7 were rejected. Additionally, claim 1 was objected to. Additionally, the drawings were objected to. Additionally, the specification was objected to. In response, Applicants hereby request reconsideration of the application in view of the amendments and the below-provided remarks. No claims are added or canceled.

For reference, claim 1 is amended to fix a minor grammatical error. In particular, claim 1 is amended to fix a misspelling of the word toroidal to refer to a toroidal spark gap cavity.

Objections to the Drawings

The Office Action states that the drawings must show every feature of the invention specified in the claims, and that the "integrated circuit" of claim 1 must be shown or the feature canceled from the claims. Applicants submit that Figure 7 is added as a new drawing in order to depict the "integrated circuit" of claim 1. Accordingly, Applicants respectfully request that the general objection to the drawings be withdrawn.

Objections to the Specification

The Office Action objects to the specification for the misspelling of the word toroidal and for referring to "interface 50." Applicants appreciate the Examiner's suggestions and submit that the specification is amended to fix each instance of a misspelling of the word "toroidal" and to remove reference to an "interface 50." Accordingly, Applicants respectfully request that the objections to the specification be withdrawn.

Objections to the Claims

The Office Action objects to claim 1 for the following informalities. In particular, claim 1 is objected to for the misspelling of the word "toroidal." Applicants submit that claim 1 is amended to present correct spellings of the word toroidal to refer to a toroidal spark gap cavity.

Claim Rejections under 35 U.S.C. 102 and 103

Claims 1, 2, 4, and 6 were rejected under 35 U.S.C. 102(b) as being anticipated by Momodomi et al. (U.S. Pat. 4,881,113, hereinafter Momodomi). Additionally, claim 7 was rejected under 35 U.S.C. 102(b) as being anticipated by El-Kareh et al. (U.S. Pat. 5,933,718, hereinafter El-Kareh). Additionally, claim 3 was rejected under 35 U.S.C. 103(a) as being unpatentable over Momodomi in view of Chen et al. (U.S. Pat. No. 5,656,534, hereinafter Chen). Additionally, claim 5 was rejected under 35 U.S.C. 103(a) as being unpatentable over Momodomi in view of Igel et al. (U.S. Pat. No. 6,204,549, hereinafter Igel). However, Applicants respectfully submit that these claims are patentable over Momodomi, El-Kareh, Chen, and Igel for the reasons provided below.

Independent Claim 1

Claim 1 recites "a pair of spaced center and circumferential electrodes, the center electrode being formed by the first electrically conductive layer and the circumferential electrode being formed by the second electrically conductive layer, said electrodes being separated by a toroidal spark gap cavity" (emphasis added). Additionally, claim 1 recites "wherein the toroid of the toroidal spark gap cavity comprises a base layer formed by the insulating layer of the integrated circuit chip" and "a cover layer formed by the dielectric layer of the integrated circuit chip, and the center of the toroid being formed by the center electrode comprising a contact pad in contact with the insulating layer" (emphasis added).

Toroidal Spark Gap Cavity

In contrast to the limitations of the claim recited above, Momodomi does not disclose a toroidal spark gap cavity between a circumferential electrode and a center electrode. Momodomi merely discloses a protrusion of a silicon dioxide layer 20 that protrudes from a layer of silicon dioxide above the layer of electrodes 17 and 18 down between the electrodes 17 and 18. Momodomi, col. 3, lines 4-7. The protrusion of silicon dioxide between the electrodes 17 and 18 is different from a toroidal spark gap cavity because a protrusion of a layer of silicon dioxide is not a cavity. Although the overall silicon dioxide layer 20 and the protrusion of the silicon dioxide layer 20 may be

enclosed, the protrusion is a portion of the overall enclosure and, hence, the protrusion is not an enclosure, or cavity, in and of itself.

Moreover, it would appear that the silicon dioxide layer 20 of Momodomi is an inter-layer dielectric to isolate the conductor 17 from the conductor 18. In the context of Momodomi, a dielectric is a non-conducting substance, i.e., an insulator. Hence, an inter-layer dielectric prevents the flow of electricity between the electrodes 17 and 18. Although an inter-layer dielectric of silicon dioxide can breakdown under a certain high voltage, and thereby pass electricity between the electrodes, the typical inter-layer dielectric is not designed for discharging electrostatic discharges because a breakdown in the silicon dioxide permanently ruins the semiconductor device. On the other hand, a spark gap cavity is designed to prevent the destruction of the semiconductor device. Hence, the silicon dioxide layer 20 of Momodomi is different from the spark gap cavity because the silicon dioxide layer 20 is an inter-layer dielectric to isolate the conductor 17 from the conductor 18. In fact, Momodomi appears to be silent with regard to an excess electric charge released through a spark gap cavity. Moreover, the protection device of Momodomi does not relate to electrostatic discharge through a spark gap cavity. Furthermore, Momodomi does not even appear to mention a break-down voltage or a spark gap cavity, or anything even related to break-down voltages or spark gap cavities.

Momodomi explains that the "n^+-type region 13 existing between the round-shaped contact hole 15 and the ring-shaped contact hole 16 acts as the resistor of the protection device as shown by the reference character R, and the PN junction forms the diode as shown by the reference character D (FIG. 2b). The protection resistor R reduces the voltage, and the diode D releases the excess electric charge to the substrate 11." Momodomi, col. 3, lines 61-68. In other words, the protection device of Momodomi involves a protection resistor R formed from the n^+-type region 13 and a diode D formed from the PN junction. Specifically, Momodomi expressly states that the excess electric charge, or the electrostatic discharge, is released through the diode D formed from the PN junction, not through the silicon dioxide layer 20, or through any purported spark gap cavity of Momodomi. Therefore, Momodomi does not disclose a spark gap cavity because Momodomi merely discloses an inter-layer dielectric between the electrodes 17 and 18.

Base Layer

Momodomi also fails to disclose a base layer formed by the insulating layer of the integrated circuit chip. Momodomi merely discloses the n^+-type region 13 that, as described above, acts as a resistor of the protection device. Moreover, the n^+-type region 13 does not make contact with the protrusion of the silicon dioxide layer 20 between the electrodes 17 and 18. Hence, the n^+-type region 13 could not possibly be understood to form a base layer of the purported spark gap cavity of Momodomi, or the silicon dioxide layer 20 because the n^+-type region 13 does not contact the purported spark gap cavity of Momodomi, the protrusion of the silicon dioxide layer 20 between the electrodes 17 and 18. Furthermore, the n^+-type region 13 is not an insulator, but an n-doped n-type semiconductor. Semiconductors are not insulators. Hence, the n^+-type region 13 does not disclose a base layer of a spark gap cavity formed by an insulating layer of the integrated circuit chip because the n^+-type region 13 region is not an insulator, and because the n^+-type region 13 does not contact the purported spark gap cavity of Momodomi, the protrusion of the silicon dioxide layer 20 between the electrodes 17 and 18.

On the other hand, if the Examiner means to suggest that the contact hole 15, of which the n^+-type region 13 is a base layer, might be the purported spark gap cavity, instead of the protrusion of the silicon dioxide layer 20 between the electrode 17 and 18, Applicants note that the contact hole 15 is merely a via, or a small opening in an insulating oxide layer that allows metallic interconnect on different interconnect layers to form an electrical connection. Momodomi explains that a "round-shaped contact hole 15 and a ring-shaped contact hole 16 are formed in the SiO_2 layer 14. A round electrode 17 and a ring-shaped electrode 18, made from A1 layers on a first level, make contact with the n^+-type region 13 through the contact holes 15 and 16, respectively." Momodomi, col. 2 line 67 through col. 3, line 4. Hence, the contact holes 15 and 16 are vias between the n^+-type region 13 and the electrodes 17 and 18, respectively. As explained above, the n^+-type region 13 acts as a resistor of the protection device to reduce the voltage of an electrostatic discharge through a diode of the PN junction. Therefore, Momodomi fails to disclose a base layer of a spark gap cavity formed by the insulating layer of the integrated circuit chip

Cover Layer

Momodomi also fails to disclose a cover layer formed by a dielectric layer of an integrated circuit chip. Momodomi merely discloses a protrusion of the silicon dioxide layer 20 between the electrodes 17 and 18. The silicon dioxide layer 20 is different from a cover layer formed by a dielectric layer because the upper layer of the silicon dioxide layer 20 is merely an extension of the protrusion of the silicon dioxide layer 20 between the electrodes 17 and 18. The silicon dioxide layer 20 and the extension of the protrusion of the silicon dioxide layer 20 between the electrodes 17 and 18 are physically the same continuous stratum of silicon dioxide that makes up the silicon dioxide layer 20. In other words, the silicon dioxide layer 20 and the protrusion of the silicon dioxide layer 20 between the electrodes 17 and 18 are the same physical element. Hence, the silicon dioxide layer 20 is not reasonably understood to be a cover layer of itself. Momodomi explains that a "CVD SiO_2 layer 20 is then deposited over the entire surface of the device." Momodomi, col. 3, lines 49 and 50. In other words, the protrusion of the silicon dioxide layer 20 between the electrodes 17 and 18 is not formed separate from the rest of the silicon dioxide layer 20, but instead is an extension of the silicon dioxide layer 20 and both are part of the same deposition process over the entire surface of the device. Therefore, Momodomi fails to disclose a cover layer formed by a dielectric layer of an integrated circuit chip.

For the reasons presented above, Momodomi does not disclose all of the limitations of the claim because Momodomi does not disclose a spark gap cavity, a base layer formed by the insulating layer of the integrated circuit chip, or a cover layer formed by the dielectric layer of the integrated circuit chip, as recited in the claim. Accordingly, Applicants respectfully assert claim 1 is not anticipated by Momodomi because Momodomi does not disclose all of the limitations of the claim.

Independent Claim 7

Claim 7 recites "depositing a first electrically conductive layer of a first electrically conductive material on said insulating layer" (emphasis added) and "depositing a dielectric layer of a dielectric material on said first electrically conductive

layer" (emphasis added). Additionally, claim 7 recites "etching spaced contact windows for a center electrode and a circumferential electrode" (emphasis added).

Depositing a Dielectric Layer

In contrast to the limitations of the claim recited above, El-Kareh does not disclose depositing a first electrically conductive layer of a first electrically conductive material on an insulating layer and depositing a dielectric layer of a dielectric material on the first electrically conductive layer. Although El-Kareh describes a polysilicon layer 152 and a silicon nitride layer 156, El-Kareh, nonetheless, fails to disclose depositing the silicon nitride layer 156 on the polysilicon layer 152. Instead, El-Kareh discloses depositing the silicon nitride layer 156 on a layer of silicide 154. El-Kareh, col. 1, lines 54-62, and Fig. 1A. Therefore, El-Kareh does not disclose depositing a first electrically conductive layer of a first electrically conductive material on an insulating layer and depositing a dielectric layer of a dielectric material on the first electrically conductive layer, as recited in the claim.

Circumferential Electrode

El-Kareh also fails to disclose a circumferential electrode. Although El-Kareh does disclose a polysilicon layer 152, El-Kareh, nonetheless, fails to disclose a circumferential electrode. Instead, El-Kareh discloses the polysilicon layer 152 as well as contact studs 170 and 178 made of some conductor. El-Kareh, col. 1, lines 54-62, col. 2, line 67 through col. 3, line 2, and Fig. 1A. However, El-Kareh appears to be silent with regard to a circumferential electrode. In fact, El-Kareh does not appear to mention any type of circumferential element. Therefore, El-Kareh does not disclose a circumferential electrode, as recited in the claim.

For the reasons presented above, El-Kareh does not disclose all of the limitations of the claim because El-Kareh does not disclose depositing a first electrically conductive layer of a first electrically conductive material on an insulating layer and depositing a dielectric layer of a dielectric material on the first electrically conductive layer. Additionally, El-Kareh does not disclose all of the limitations of the claim because El-Kareh does not disclose a circumferential electrode, as recited in the claim. Accordingly, Applicants respectfully assert claim 7 is not anticipated by El-Kareh because El-Kareh does not disclose all of the limitations of the claim.

Dependent Claims

Claims 2-6 depend from and incorporate all of the limitations of independent claim 1. Applicants respectfully assert claims 2-6 are allowable based on an allowable base claim. Additionally, each of claims 2-6 may be allowable for further reasons.

CONCLUSION

Applicants respectfully request reconsideration of the claims in view of the amendments and remarks made herein. A notice of allowance is earnestly solicited.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-3444** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-3444** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

/mark a. wilson/

Date: June 11, 2008

Mark A. Wilson
Reg. No. 43,994

Wilson & Ham
PMB: 348
2530 Berryessa Road
San Jose, CA 95132
Phone: (925) 249-1300
Fax: (925) 249-0111